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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/781,125	02/18/2004	Christopher S. Johnson	400.149US02	3355

27073 7590 01/20/2006

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EXAMINER	
LE, THONG QUOC	

ART UNIT	PAPER NUMBER
2827	

DATE MAILED: 01/20/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/781,125	JOHNSON, CHRISTOPHER S.	
	Examiner	Art Unit	
	Thong Q. Le	2827	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 November 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-44* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-44* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Amendment filed on 11/14/2005 has been entered.

2. Claims 1-44 are presented for examination.

Response to Arguments

3. Applicant's arguments with respect to claims 1-44 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 1,4-5,16,22-23,27,30-31 are rejected under 35 U.S.C. 102(b) as being anticipated by Ingalls (U.S. Patent No. 5,978,297).

Regarding claim 1, Ingalls discloses a system (Figure 6, 320), comprising:

a controller (Figure 6, 322); and

a memory device (Figure 6, 321) coupled to the controller to receive signals therefrom (Figure 6, 336), and comprising:

an array of memory cells (Figure 1, 20, 22) arranged in a plurality of addressable banks (Figure 1, 14, BA, Column 1, lines 11-22), each bank comprises addressable rows and columns of memory cells (Figure 1, 40, 26, Column 1, lines 25-37);

a mode register (Figure 1, 69, Column 1, line 60); and

address circuitry (Figure 1, 18, Column 1, lines 17-46) coupled to the mode register to configure the addressable banks in response to a program state of the mode register (Column 2, lines 50-56, Column 5, lines 13-20).

Regarding claims 4-5, Ingalls discloses a system (Figure 6, 320) , comprising a controller (322) ; and

a dynamic random access memory device (321) coupled to the controller and comprising:

an array of X memory cells (Figure 1, 20, 22);

a mode register (Figure 1, 69) ; and

address circuitry (Figure 1, 18, Column 1, lines 17-46) coupled to the mode register to configured the array in response to a program state of the mode register, wherein the mode register defines a number of addressable banks of the array (Column 5, lines 50-60), and wherein a first state of the mode register configures the array into Y banks each having X/Y memory cells, and a second state of the mode register configures the array into Z bank each having X/Z memory cells (Figure 1, bank 0, bank 1, Column 1, lines 1-32, lines 47-57).

Regarding claims 16, 22-23, 27, 30-31, Ingalls discloses a system, comprising a controller (Figure 16, 322), and a memory device (Figure 16, 321) coupled to the controller to receive signals (Figure 16, 336) including an input signal therefrom, and comprising an array of memory cells (Figure 1, 20, 22) arranged in a plurality of addressable banks, each bank comprises addressable rows and columns of memory cells (Figure 1) ; a decode circuit (Figure 1, 28) to decode the input signal; and address

circuitry (Figure 1, 18) coupled to the decode circuit to configure the addressable banks in response to a program state of the input signal (Column 2, lines 50-56, Column 5, lines 13-20), and wherein a first state of the mode register configures the array into Y banks each having X/Y memory cells, and a second state of the mode register configures the array into Z bank each having X/Z memory cells (Figure 1, bank 0, bank 1, Column 1, lines 1-32, lines 47-57).

6. Claims 1-44 are rejected under 35 U.S.C. 102(b) as being anticipated by Ooishi (U.S. Patent No. 6,084,818).

Regarding claim 1-3, Ooishi discloses a system (Figure 1), comprising a controller (Column 1, lines 12-13) and a memory device (Figure 1, 1000) coupled to the controller to receive signals therefrom, and comprising an array of memory cells (Figure 1, 1100) arranged in a plurality of addressable banks (Figure 1, 1052) , each bank comprises addressable rows and columns of memory cells (Figure 1, 1048, 1050), a mode register (Figure 1, 1046), and address circuitry coupled to the mode register to configure the addressable banks in response to a program state of the mode register (Column 5, lines 46-67, Column 6, lines 1-11), and wherein the addressable banks can be configured as either four or eight banks (Figure 1, Column 6, lines 19-44, Figure 30, GR1-GR4), and wherein the address circuitry selectively routes address signal to either a row decoder (Figure 1, 2142) or a bank decoder (Figure 1, 1066) in response to the mode register.

Regarding claims 4-8, Ooishi discloses a system (Figure 1) , comprising a controller (Column 1, lines 12-13), and a dynamic random access memory device

(Figure 1, 1000) coupled to the controller and comprising an array of X memory cells (Figure1, 1100), a mode register (Figure 1, 1046), and address circuitry (Figure 1, 1050, 1052) coupled to the mode register to configured the array in response to a program state of the mode register (Column 6, lines 1-11), and wherein the mode register defines a number of addressable banks of the array (Column 6, lines 1-44), and wherein a first state of the mode register configures the array into Y banks each having X/Y memory cells, and a second state of the mode register configures the array into Z banks each having X/Z memory cells (Column 6, lines 38-44), and wherein the address circuitry comprises column (Figure 1, 2104) , row (Figure 1, 2142) and bank address decoders (Figure 1, 1066), and wherein the address circuitry (Figure 1, 1058) routes a selected address input signal to either the row or bank decoder in response to the mode register (figure 1, Column 5, lines 45-67, Column 6, lines 1-18), and wherein the address circuitry comprises a multiplex circuit (Figure 1, 1058).

Regarding claims 9-11, 12-15, 22-26, 27-29, 30-34, 35-41, Ooishi discloses a system (Figure 1), comprising a controller (Column 1, lines 12-13) and a synchronous dynamic random access memory (SDRAM) (Column 1, lines 12-16) coupled to the controller and comprising an array of X memory cells (Figure 1, 1100), a mode register (Figure 1, 1046) ; a column address decoder (Figure 1, 2104) ; a row address decoder (Figure 1, 2142) ; a bank address decoder (Figure 1, 1066), and address signal circuitry (Figure 1, 1058) coupled to a plurality of address signal input (Figure 1, 1030) connections the address signal circuitry routes a selected one of the plurality of address input connections to either the row or bank address decoder in response to data stored

in the mode register (Column 5, lines 46-67, Column 6, lines 1-11), and wherein a first state of the mode register configures the array into Y banks each having X/Y memory cells, and a second state of the mode register configures the array into Z banks each having X/Z memory cells (Column 5, lines 46-67, Column 6, lines 1-18), and wherein X = 4 and Z = 8 (Column 6, lines 38-43), and wherein the at least one external input connection comprises two input connections to receive a two-bit configuration signal (Figure 14, Column 14, lines 56-67).

Regarding claims 16-21, Ooishi discloses a system (Figure 1), comprising a controller (Column 1, lines 12-13); and a memory device (Figure 1) coupled to the controller to receive signals (Figure1, 1030) including an input signal therefrom, and comprising an array of memory cells (Figure 1, 1100) arranged in a plurality of addressable banks (figure 1) , each bank comprises addressable rows and columns of memory cells (Figure 1) ; a decode circuit (Figure 1, 2142) to decode the input signal; and address circuitry (Figure 1, 1058) coupled to the decode circuit to configure the addressable banks in response to a program state of the input signal (Column 5, lines 46-67, Column 6, lines 1-18), and wherein the addressable banks can be configured as either four or eight banks (Figure 30, GR1-GR4), and wherein the address circuitry selectively routes address signal to either a row decoder (Figure 1, 2142) or a bank decoder (figure 1, 1066) in response to the input signal (Column 6, lines 1-37), and wherein the input signal is a one-bit binary input (Column 5, lines 54-55), and wherein the input signal is a multi-bit binary input (Column 5, lines 54-55) and the number of

banks is configurable (Column 54-67, column 6, lines 1-11), and wherein the number of banks is four or eight (Figure 30, GR1-GR4).

Regarding claims 42-44, the apparatus discussed above would perform the method in claims 42-44.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thong Q. Le whose telephone number is 571-272-1783. The examiner can normally be reached on 8:00am-5:00pm M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Zarabian Amir can be reached on 571-272-1852. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Thong Q. Le
Primary Examiner
Art Unit 2827

1/17/2006